CLAIMS

I claim:

1. A circuit for sensing a voltage across a power switch, said power switch having a first current handling terminal, a second current handling terminal and a control terminal receiving a first control signal, said first control signal turning said power switch on and off to generate a switching voltage at said first current handling terminal, said circuit comprising:

a transmission gate having an input terminal coupled to said first current handling of said power switch, an output terminal, and a control terminal, said control terminal coupled to receive a signal corresponding to said first control signal such that said transmission gate is turned on whenever said power switch is turned on, said output terminal providing a sampled voltage indicative of the voltage across said power switch when said power switch is turned on;

a low pass filter having an input terminal coupled to said output terminal of said transmission gate and an output terminal providing a filtered voltage; and

a comparator having a first and second input terminals coupled to receive said filtered voltage and a reference voltage, said comparator providing an output signal having a first value when said filtered voltage is less than said reference voltage and a second value when said filtered voltage is greater than said reference voltage.

2. The circuit of claim 1, wherein said power switch comprises an NMOS transistor having a drain terminal being said first current handling terminal and coupled to a second power

switch, a source terminal being said second current handling terminal and coupled to a first supply voltage and a gate terminal being said control terminal, and wherein said NMOS transistor and said second power switch are turned on alternately to generate said switching voltage at said drain terminal of said NMOS transistor, said NMOS transistor turning on to cause said switching voltage to decrease while the second power switch turning on to cause said switching voltage to increase.

3. The circuit of claim 1, wherein said power switch comprises a PMOS transistor having a drain terminal being said first current handling terminal and coupled to a second power switch, a source terminal being said second current handling terminal and coupled to a first supply voltage and a gate terminal being said control terminal, and wherein said PMOS transistor and said second power switch are turned on alternately to generate said switching voltage at said drain terminal of said PMOS transistor, said PMOS transistor turning on to cause said switching voltage to increase while the second power switch turning on to cause said switching voltage to decrease.

4. The circuit of claim 1, wherein said transmission gate comprises an NMOS transistor and a PMOS transistor connected in parallel between the input terminal and the output terminal of said transmission gate, the gate terminal of said NMOS transistor is driven by a second control signal corresponding to said first control signal and the gate terminal of said PMOS transistor is driven by a signal corresponding to an inverse of said second control signal.

5. The circuit of claim 1, wherein said low pass filter comprises a resistor-capacitor (*RC*) filter network.

6. The circuit of claim 5, wherein said resistor-capacitor (RC) filter network comprises:

a first resistor coupled between said output terminal of said transmission gate and a first node; and

a capacitor coupled between said first node and a first supply voltage.

7. The circuit of claim 1, wherein said comparator comprises a hysteresis comparator and said reference voltage comprises a first voltage value and a second, larger voltage value, and wherein said reference voltage is set to said second, larger voltage value when said output signal has said first value, and said reference voltage is set to said first voltage value when said reference voltage has said second value.

8. An output circuit for a switching regulator comprising:

a first power switch and a second power switch connected in series between a first supply voltage and a second supply voltage;

a driver circuit receiving a switch control signal and generating a first control signal and a second control signal corresponding to said switch control signal for driving said first power switch and said second power switch, respectively, said driver circuit causing said first power switch and said second power switch to turn on alternately for generating a switching voltage at a switch node between said first power switch and said second power switch; and

a load sensing circuit for sensing the load condition driven by said first power switch and said second power switch, said load sensing circuit comprising:

a transmission gate having an input terminal coupled to said switch node of said first and second power switches, an output terminal, and a control terminal, said control terminal coupled to receive a signal corresponding to said second control signal driving said second power switch such that said transmission gate is turned on whenever said second control signal is asserted to turn said second power switch on, said output terminal providing a sampled voltage indicative of the voltage across said second power switch when said second power switch is turned on;

a low pass filter having an input terminal coupled to said output terminal of said transmission gate for low pass filtering said sampled voltage and an output terminal providing a filtered voltage; and

a comparator having a first and a second input terminals coupled to receive said filtered voltage and a reference voltage, said comparator providing an output signal having a first value when said filtered voltage is less than said reference voltage and a second value when said filtered voltage is greater than said reference voltage.

9. The circuit of claim 8, wherein said second power switch comprises an NMOS transistor having a drain terminal coupled to said switch node, a source terminal coupled to said second supply voltage and a gate terminal being driven by said second control signal.

10. The circuit of claim 9, wherein said first power switch comprises a PMOS transistor having a drain terminal coupled to said switch node, a source terminal coupled to said first supply voltage and a gate terminal being driven by said first control signal.

11. The circuit of claim 8, wherein said transmission gate comprises an NMOS transistor and a PMOS transistor connected in parallel between the input terminal and the output terminal of said transmission gate, the gate terminal of said NMOS transistor being driven by a third control signal corresponding to said second control signal and the gate terminal of said PMOS transistor being driven by a signal corresponding to an inverse of said third control signal.

12. The circuit of claim 8, wherein said low pass filter comprises a resistor-capacitor (*RC*) filter network.

13. The circuit of claim 12, wherein said resistor-capacitor (RC) filter network comprises:

a first resistor coupled between said output terminal of said transmission gate and a first node; and

a capacitor coupled between said first node and a first supply voltage.

14. The circuit of claim 8, wherein said comparator comprises a hysteresis comparator and said reference voltage comprises a first voltage value and a second, larger voltage value, and wherein said reference voltage is set to said second, larger voltage value when said output signal has said first value, and said reference voltage is set to said first voltage value when said reference voltage has said second value.

15. The circuit of claim 8, wherein said second power switch comprises a first NMOS transistor and a second NMOS transistor connected in parallel between said switch node and said second supply voltage, said second NMOS transistor being smaller than said first MOS transistor, and wherein said second NMOS transistor is driven by a signal corresponding to said second control signal and said first NMOS transistor is driven by a fourth control signal corresponding to said switch control signal and said output signal of said comparator such that said first NMOS transistor is turned off when said output signal of said comparator has said first value.

16. The circuit of claim 15, wherein said first power switch comprises a first PMOS transistor and a second PMOS transistor connected in parallel between the first supply voltage and said switch node, said second PMOS transistor being smaller than said first PMOS transistor, and wherein said second PMOS transistor is driven by a signal corresponding to said first control signal and said first PMOS transistor is driven by a fifth control signal corresponding to said switch control signal and said output signal of said comparator, such that said first PMOS transistor is turned off when said output signal of said comparator has said first value.

17. The circuit of claim 15, wherein the first NMOS transistor is ten times larger than the second NMOS transistor.

18. The circuit of claim 16, wherein the first PMOS transistor is ten times larger than the second PMOS transistor.

19. An output circuit for a switching regulator comprising:

a first power switch and a second power switch connected in series between a first supply voltage and a second supply voltage;

a driver circuit receiving a switch control signal and generating a first control signal and a second control signal corresponding to said switch control signal for driving said first power switch and said second power switch, respectively, said driver circuit causing said first power switch and said second power switch to turn on alternately for generating a switching voltage at a switch node between said first power switch and said second power switch; and

a load sensing circuit for sensing the load condition driven by said first power switch and said second power switch, said load sensing circuit comprising:

a transmission gate having an input terminal coupled to said switch node of said first and second power switches, an output terminal, and a control terminal, said control terminal coupled to receive a signal corresponding to said first control signal driving said first power switch such that said transmission gate is turned on whenever said first control signal is asserted to turn said first power switch on, said output terminal providing a sampled voltage indicative of the voltage across said first power switch when said first power switch is turned on;

a low pass filter having an input terminal coupled to said output terminal of said transmission gate for low pass filtering said sampled voltage and an output terminal providing a filtered voltage; and

a comparator having a first and a second input terminals coupled to receive said filtered voltage and a reference voltage, said comparator providing an output signal having a first value when said filtered voltage is greater than said reference voltage and a second value when said filtered voltage is less than said reference voltage.

20. The circuit of claim 19, wherein said first power switch comprises a PMOS transistor having a drain terminal coupled to said switch node, a source terminal coupled to said first supply voltage and a gate terminal being driven by said first control signal.

21. The circuit of claim 20, wherein said second power switch comprises an NMOS transistor having a drain terminal coupled to said switch node, a source terminal coupled to said second supply voltage and a gate terminal being driven by said second control signal.

22. A method for sensing a voltage across a power switch, said power switch having a first current handling terminal, a second current handling terminal and a control terminal receiving a first control signal, said first control signal turning said power switch on and off to generate a switching voltage at said first current handling terminal, said method comprising:

sampling a voltage at said power switch when said power switch is turned on;

filtering the sampled voltage to remove high frequency components;

comparing the filtered voltage to a reference voltage;

generating an output signal having a first value when said filtered voltage is less than said reference voltage and a second value when said filtered voltage is greater than said reference voltage.

23. The method of claim 22, wherein said sampling a voltage at said power switch comprises:

coupling a transmission gate to said first current handling of said power switch; and

turning on said transmission gate in response to said first control signal, such that said transmission gate samples said voltage across said power switch when said power switch is turned on.

24. The method of claim 22, wherein said reference voltage has a first voltage value and a second, larger voltage value, said method further comprises:

selecting said second voltage value for said reference voltage when said output signal has said first value; and

selecting said first voltage value for said reference voltage when said output signal has said second value.